REMARKS

This paper is being provided in response to the Office Action mailed February 13, 2004, for the above-referenced application. In this response, Applicant has amended claims 1 and 6 to clarify that which Applicant considers to be the invention. Applicant respectfully submits that the amendments to the claims are fully supported by the originally-filed specification.

The rejection of claims 1-11 and 20-23 under 35 U.S.C. 112, second paragraph, as being indefinite is addressed by amendments to the claims contained herein. The Office Action questions the phrase "with said first drain and source diffusion layers surrounding said second drain and source diffusion layers on at least a bottom and a lateral side." Applicants have amended the feature to recite "wherein said at least one first drain and source diffusion layer contacts said at least one second drain and source diffusion layer on at least a bottom and a lateral side." Applicants respectfully submit that the claimed features of at least one second drain formed at a surface of said semiconductor substrate around said gate electrode and a first drain and source diffusion layer that contacts the second drain and source diffusion layer on at least a bottom and a lateral side is definite and clearly disclosed and recited. (See, for example, elements 63, 64, 65 and 66 of Figure 3 of the present specification.) Applicant respectfully submits that this feature would be understood by one of ordinary skill in the art and respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of claims 1, 3-6, 9-11, 20 and 22 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,439,835 to Gonzalez (hereinafter "Gonzalez") in view of U.S. Patent No. 5,545,575 to Cheng et al. (hereinafter "Cheng") is hereby traversed and

reconsideration is respectfully requested in view of the amendments to the claims contained herein.

Independent claim 1, as amended herein, recites a semiconductor device including a semiconductor substrate, an insulating film formed at a surface of the semiconductor substrate for defining device regions in each of which a semiconductor device is to be fabricated, and a gate electrode formed on the semiconductor substrate, the gate electrode and the insulating film defining at least one lightly doped first drain and source diffusion layer. At least one sidewall covers the gate electrode. At least one second drain and source diffusion layer is formed at a surface of the substrate and contacted by the first drain and source diffusion layer on at least a bottom and a lateral side. The sidewall has a sidewall offset connected thereto and extending by more than the thickness of the sidewall. The lightly doped first drain and source diffusion layer extends towards the gate electrode beyond an edge of the sidewall offset, and the heavily doped second drain and source diffusion layer extends below said sidewall offset but is spaced outwardly away from an edge of the gate electrode in a direction along said surface of said semiconductor substrate. Further, all of the at least one second drain and source diffusion layer that is exposed to said surface of said semiconductor substrate has a lateral dimension along the surface of said semiconductor substrate that is approximately equal to and aligned with the lateral dimension of said sidewall offset. Claims 2-5, 20 and 21 depend directly or indirectly on independent claim 1.

Independent claim 6, as amended herein, recites a semiconductor device including a semiconductor substrate, an insulating film formed at a surface of the semiconductor substrate

for defining device regions in each of which a semiconductor device is to be fabricated, and a gate electrode formed on the semiconductor substrate, the gate electrode and the insulating film defining at least one lightly doped first drain and source diffusion layer. There is at least one sidewall covering the gate electrode, and at least one heavily doped second drain and source diffusion layer formed at a surface of the semiconductor substrate around the gate electrode, wherein the first drain and source diffusion layer contacts the second drain and source diffusion layer on at least a bottom and a lateral side. The sidewall has a sidewall offset connected thereto and extending outwardly of the gate electrode along the surface of the semiconductor substrate in at least one region below which the at least one second drain and source diffusion layer is formed. The sidewall offset extends along a lateral surface of the gate oxide film on which the gate electrode is formed by an amount that is greater than the thickness of the sidewall. Low-resistive wiring layers are formed at the surface of the drain and source diffusion layers and located outwardly beyond a peripheral edge of the sidewall and offset in at least one drain and source diffusion layer. The lightly doped first drain and source diffusion layer extends towards the gate electrode beyond an edge of the sidewall offset, and the heavily doped second drain and source diffusion layer extends below said sidewall offset but are spaced outwardly away from an edge of the gate electrode in a direction along said horizontal surface of said semiconductor substrate. Further, all of said at least one second drain and source diffusion layer that is exposed to said surface of said semiconductor substrate has a lateral dimension along the surface of said semiconductor substrate that is approximately equal to and aligned with the lateral dimension of said sidewall offset. Claims 7-11, 22 and 23 depend directly or indirectly on independent claim 6.

The Gonzalez reference discloses a process for fabricating a CMOS DRAM using a high energy ion implantation of boron ions at a oblique angle for punch through protection. The graded junction 24B is formed by the oblique implantation. The junction of the diffusion is not aligned to the edge of the sidewall offset over gates 16 and 17. (See Abstract and Figures 8 and 9 of Gonzalez).

The Cheng reference discloses an insulated gate semiconductor device having gate electrodes, and a source region 57 nested inside source region 43, etc. Openings in a layer of dielectric material 63 expose portions of the source/drain diffusion regions to form silicide 64. Cheng is used in the Office Action to show that first source/drain diffusion regions may surround second source/drain diffusion regions and have different diffusion concentrations. (See Abstract; col. 5, lines 39-67; and Figure 7 of Cheng).

Applicant's independent claims, as amended herein, all recite a semiconductor device having at least the feature of at least one lightly doped first drain and source diffusion layer extending towards said gate electrode beyond an edge of said sidewall offset, and at least one heavily doped second drain and source diffusion layer extending below said sidewall offset but spaced outwardly away from an edge of the gate electrode in a direction along said horizontal surface of said semiconductor substrate, and *wherein all of said at least one second drain and source diffusion layer that is exposed to said surface of said semiconductor substrate has a lateral dimension along the surface of said semiconductor substrate that is approximately equal to and aligned with the lateral dimension of said sidewall offset.* Applicant has clarified herein the alignment relationship between the second drain and source diffusion layer and the sidewall

offset. The sidewall offset prevents the second diffusion layer from being exposed at a surface of the semiconductor substrate and, accordingly, it is possible to prevent the low-resistive wiring layer from abnormally growing above the second diffusion layer. In addition, since the sidewall offset is formed only above the second drain and source diffusion layer, unnecessary increase of a chip area is prevented. This structure of the present claimed invention makes it possible for the source and drain diffusion layers, by being outwardly spaced away from the edge of the gate electrode of a transistor, to have a high breakdown voltage and thereby prevents generation of a leakage current between bands. (See, for example, page 9, lines 11-24; and Figures 3 and 4 of the present application, particularly gate electrode element 52, sidewall 53, sidewall offset 54, and layers 63-66.)

Applicant respectfully submits that neither Gonzalez nor Cheng, taken alone or in any combination, teach or suggest at least the above features as claimed by Applicant. Specifically, Gonzalez discloses a gate electrode, sidewall and sidewall offset and drain and source regions (see, for example, Figure 9 of Gonzalez), but the sidewall of Gonzalez below which are positioned multiple drain and source regions does NOT include a sidewall offset. Consequently, Gonzalez contains no disclosure of a sidewall offset (nor even the sidewall) that is aligned with the second drain and source diffusion layer and *wherein all of said at least one second drain and source diffusion layer that is exposed to said surface of said semiconductor substrate has a lateral dimension along the surface of said semiconductor substrate that is approximately equal to and aligned with the lateral dimension of said sidewall offset.* Gonzalez does not appear to recognize the advantages of this configuration of first and second source diffusion layers with respect to the gate electrode, sidewall and sidewall offset that enhances breakdown voltage,

reduces leakage current, and prevents abnormal wiring layer growth and unnecessary increases in chip area.

Applicant respectfully submits that Cheng fails to overcome the above-noted deficiencies of Gonzalez with respect to Applicant's claimed invention. Cheng discloses a polysilicon plug 28 to which is attached gate electrode extension material portions 49 and 52 and first and second dopant regions 43, 44 and 57, 58. (See col. 5, lines 39-67 of Cheng). Cheng's dopant regions 57 and 58 extend below so as to overlap vertically with the gate electrode portions 49 and 52, but there is no alignment nor equalized dimensions of a sidewall offset with respect to the portion of a source and drain diffusion layer that is exposed to the substrate surface. For example, in Figure 7 of Cheng, the dopant regions, such as regions 57 and 58 extend beyond the peripheral edges of the sidewalls. Applicant notes that this configuration does not achieve the advantages, such as preventing unnecessary increases in chip area, that are provided by Applicant's claimed invention.

Applicant respectfully submits that neither Gonzalez nor Cheng, taken alone or in any combination, teach or fairly suggest a semiconductor device having at least the feature of at least one lightly doped first drain and source diffusion layer extending towards said gate electrode beyond an edge of said sidewall offset, and at least one heavily doped second drain and source diffusion layer extending below said sidewall offset but spaced outwardly away from an edge of the gate electrode in a direction along said horizontal surface of said semiconductor substrate, and *wherein all of said at least one second drain and source diffusion layer that is exposed to said surface of said semiconductor substrate has a lateral dimension along the surface of said*

semiconductor substrate that is approximately equal to and aligned with the lateral dimension of said sidewall offset, as is claimed by Applicant. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of claim 7 under 35 U.S.C. 103(a) as being unpatentable over Gonzalez in view of Cheng and further in view of U.S. Patent No. 5,316,977 to Kunishima et al. (hereinafter "Kunishima") is hereby traversed and reconsideration is respectfully requested.

Claim 7 depends from independent claim 6, discussed above, and recites that low-resistive wiring layers are composed of TiSi.

The Gonzalez and Cheng references are discussed above.

The Kunishima reference is cited by the Office Action as disclosing a silicide layer comprising titanium silicide, using a semiconductor device as a CMOS device, and a sidewall entirely covering the gate electrode.

Applicant respectfully submits that Kunishima fails to overcome the above-noted deficiencies of the Gonzalez and Cheng references with respect to Applicant's claimed invention. Applicant respectfully submits that neither Kunishima, Gonzalez nor Cheng, taken alone or in any combination, teach or fairly suggest a semiconductor device having at least the feature of at least one lightly doped first drain and source diffusion layer extending towards said gate electrode beyond an edge of said sidewall offset, and at least one heavily doped second drain and

source diffusion layer extending below said sidewall offset but spaced outwardly away from an edge of the gate electrode in a direction along said horizontal surface of said semiconductor substrate, and *wherein all of said at least one second drain and source diffusion layer that is exposed to said surface of said semiconductor substrate has a lateral dimension along the surface of said semiconductor substrate that is approximately equal to and aligned with the lateral dimension of said sidewall offset*, as is claimed by Applicant. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of claims 1-4, 8-10, 21 and 23 under 35 U.S.C. 103(a) as being unpatentable over Cheng is hereby traversed and reconsideration is respectfully requested.

Claims 2-3, 8-10, 21 and 23 depend on independent claims 1 and 6, discussed above.

The Cheng reference is discussed above with respect to Applicant's claims. As noted, Applicant respectfully submits that Cheng does not teach or fairly suggest a semiconductor device having at least the feature of at least one lightly doped first drain and source diffusion layer extending towards said gate electrode beyond an edge of said sidewall offset, and at least one heavily doped second drain and source diffusion layer extending below said sidewall offset but spaced outwardly away from an edge of the gate electrode in a direction along said horizontal surface of said semiconductor substrate, and *wherein all of said at least one second drain and source diffusion layer that is exposed to said surface of said semiconductor substrate has a lateral dimension along the surface of said semiconductor substrate that is approximately equal*

to and aligned with the lateral dimension of said sidewall offset, as is claimed by Applicant. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of claims 5, 7, 11, 21 and 23 under 35 U.S.C. 103(a) as being unpatentable over Cheng in view of Kunishima is hereby traversed and reconsideration is respectfully requested.

Claims 5, 7, 11, 21 and 23 depend on independent claims 1 and 6, discussed above.

The Cheng and Kunishima references are discussed above.

Applicant respectfully submits that neither Cheng nor Kunishima, taken alone or in any combination, teach or fairly suggest a semiconductor device having at least the feature of at least one lightly doped first drain and source diffusion layer extending towards said gate electrode beyond an edge of said sidewall offset, and at least one heavily doped second drain and source diffusion layer extending below said sidewall offset but spaced outwardly away from an edge of the gate electrode in a direction along said horizontal surface of said semiconductor substrate, and *wherein all of said at least one second drain and source diffusion layer that is exposed to said surface of said semiconductor substrate has a lateral dimension along the surface of said semiconductor substrate that is approximately equal to and aligned with the lateral dimension of said sidewall offset*, as is claimed by Applicant. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

Based on the above, Applicants respectfully request that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-248-4038.

Respectfully submitted,
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